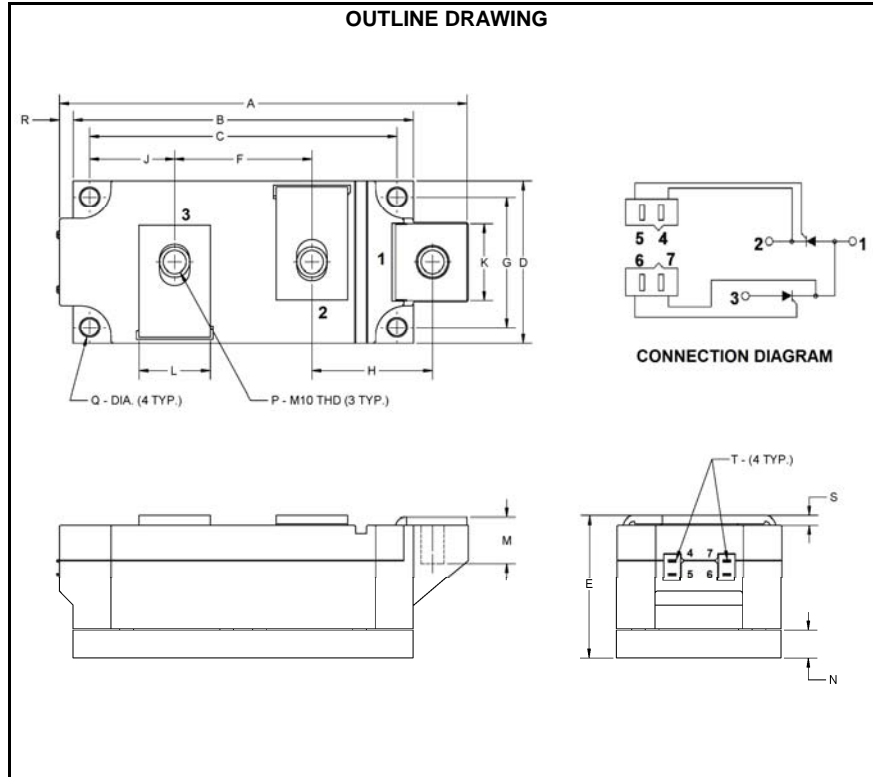


POW-R-BLOK™
Dual SCR Isolated Module
500 Amperes / 1600 to 1800 Volts



LDR3_50
Dual SCR
POW-R-BLOK™ Module
500 Amperes / 1600-1800 Volts

Description:

Powerex Dual SCR Modules are designed for use in applications requiring phase control and isolated packaging. The modules are isolated for easy mounting with other components on a common heatsink. *POW-R-BLOK™* has been tested and recognized by the Underwriters Laboratories.

Features:

- Electrically Isolated Heatsinking
- Compression Bonded Elements
- Metal Baseplate
- Low Thermal Impedance for Improved Current Capability
- Includes Gate Lead Kits and M10 Terminal Hardware
- UL Recognized (E78240)
- RoHS Compliant

Benefits:

- No Additional Insulation Components Required
- Easy Installation
- No Clamping Components Required
- Reduce Engineering Time

Applications:

- Bridge Circuits
- AC & DC Motor Drives
- Battery Supplies
- Power Supplies
- Large IGBT Circuit Front Ends

Ordering Information:

Select the complete eight-digit module part number from the table below.

Example: LDR31650 is a 1600V, 500 Ampere Dual SCR Isolated *POW-R-BLOK™* Module.

Type	Voltage Volts (x100)	Current Amperes (x10)
LDR3	16 18	50

LDR3 Outline Dimensions

Dimension	Inches	Millimeters
A	5.87	149
B	4.88	124
C	4.41	112
D	2.36	60
E	2.05	52
F	1.97	50
G	1.89	48
H	1.73	44
J	1.22	31
K	1.10	28
L	1.02	26
M	0.67	17
N	0.39	10
P	M10 Metric	M10
Q	0.26 Dia.	6.5 Dia.
R	0.20	5
S	0.12	3
T	.110 x .032	2.8 x 0.8

Note: Dimensions are for reference only.

Absolute Maximum Ratings

Characteristics	Conditions	Symbol		Units
Repetitive Peak Forward and Reverse Blocking Voltage		V_{DRM} & V_{RRM}	up to 1800	V
Non-Repetitive Peak Blocking Voltage ($t < 5$ msec)		V_{RSM}	$V_{RRM} + 100$	V
RMS Forward Current	180° Conduction, $T_C=85^\circ\text{C}$, 50 Hz	$I_{T(RMS)}$	785	A
Average Forward Current	180° Conduction, $T_C=85^\circ\text{C}$, 50 Hz	$I_{T(AV)}$	500	A
Peak One Cycle Surge Current, Non-Repetitive	60 Hz, 0V reappplied, $T_j = T_{j\max}$	I_{TSM}	17,000	A
	60 Hz, 0V reappplied, $T_j = 25^\circ\text{C}$	I_{TSM}	20,000	A
	50 Hz, 0V reappplied $T_j = T_{j\max}$	I_{TSM}	15,500	A
	50 Hz, 0V reappplied, $T_j = 25^\circ\text{C}$	I_{TSM}	18,000	A
I^2t for Fusing for One Cycle	60 Hz, 0V reappplied, $T_j = T_{j\max}$	I^2t	1.19×10^6	A^2sec
	60 Hz, 0V reappplied, $T_j = 25^\circ\text{C}$	I^2t	1.66×10^6	A^2sec
	50 Hz, 0V reappplied $T_j = T_{j\max}$	I^2t	1.20×10^6	A^2sec
	50 Hz, 0V reappplied, $T_j = 25^\circ\text{C}$	I^2t	1.62×10^6	A^2sec
Average Forward Gate Power		$P_{G(AV)}$	4	W
Maximum Rate-of-Rise of On-State Current, (Repetitive)	$T = T_{j\max}$, $V_D = 0.67 V_{DRM}$, $I_{TM} = 2 I_{TAV}$, Gate Pulse: $I_G = 2$ A, $t_{GP} = 50 \mu\text{s}$, $di_G/dt \geq 1$ A/ μs	di/dt	400	A/ μs
Operating Temperature		T_j	-40 to +130	$^\circ\text{C}$
Storage Temperature		T_{stg}	-40 to +125	$^\circ\text{C}$
Max. Mounting Torque, M6 Mounting Screw			55	in. – Lb.
			6	Nm
Max. Mounting Torque, M10 Terminal Screw			110	in. – Lb.
			12	Nm
Module Weight, Typical			1.5	kg
			3.30	lb
V Isolation @ 25C	$t = 1$ minute, 50 Hz	V_{rms}	3000	V

Information presented is based upon manufacturers testing and projected capabilities.
 This information is subject to change without notice.
 The manufacturer makes no claim as to the suitability of use, reliability, capability,
 or future availability of this product.

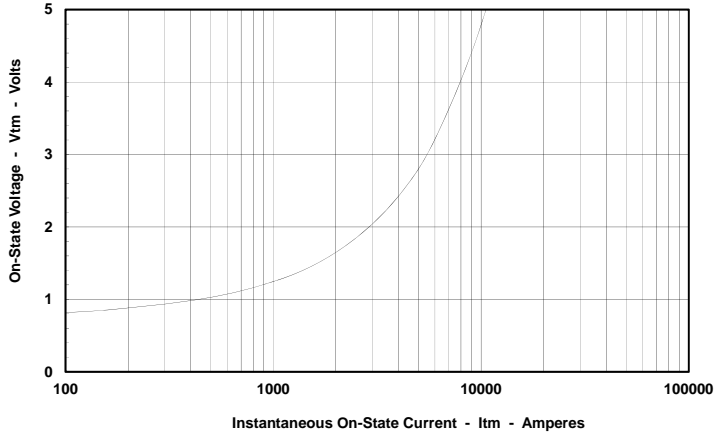
Electrical Characteristics, T_J=25°C unless otherwise specified

Characteristics	Symbol	Test Conditions	Min.	Max.	Units
Repetitive Peak Forward Leakage Current	I _{DRM}	V _D = V _{DRM} , T _J = 130°C		70	mA
Repetitive Peak Reverse Leakage Current	I _{RDM}	V _R = V _{RDM} , T _J = 130°C		70	mA
Peak On-State Voltage	V _{FM}	I _{TM} = 1570A		1.50	V
Threshold Voltage, Low-level	V _{(TO)1}	T _J = 130°C, I = 0.5 I _{T(AV)} to 1.5 I _{T(AV)}		0.85	V
Slope Resistance, Low-level	r _{T1}			0.40	mΩ
V _{TM} Coefficients, Full Range		T _J = 130°C, I = 0.5 I _{T(AV)} to 1.5 I _{T(AV)} V _{TM} = A + B Ln I + C I + D Sqrt I	A = B = C = D =	-2.5548 0.8017 9.55E-04 -0.0851	
Critical Rate of Rise of Off-State Voltage	dV/dt	V _D = 0.67 V _{DRM} , T _J = 130°C, Gate Open		1000	V/μs
Gate Trigger Current	I _{GT}	T _J = 25°C, V _D = 12V		250	mA
Gate Trigger Voltage	V _{GT}	T _J = 25°C, V _D = 12V		2.5	V
Non-Triggering Gate Voltage	V _{GDM}	T _J = 130°C, V _D = 0.67 V _{DRM}		0.25	V
Peak Forward Gate Current	I _{GTM}			4.0	A
Peak Reverse Gate Voltage	V _{GDM}			5	V
Latching Current	I _L	T _J = 25 °C, V _D = 12 V, Gate Pulse: I _G = 2 A, t _{GP} = 50 μs, di _G /dt >= 1 A/μs		1000	mA
Holding Current	I _H	T _J = 25 °C, V _D = 0.67 V _{DRM} , Gate Open		300	mA
Turn-Off Time	t _q	I _{TM} = I _{T(AV)} , di/dt = 10 A/us, dV _D /dt = 50 V/us, V _D = 0.67 V _{DRM} , V _R = 100 V, T _J = 130°C		250	μs

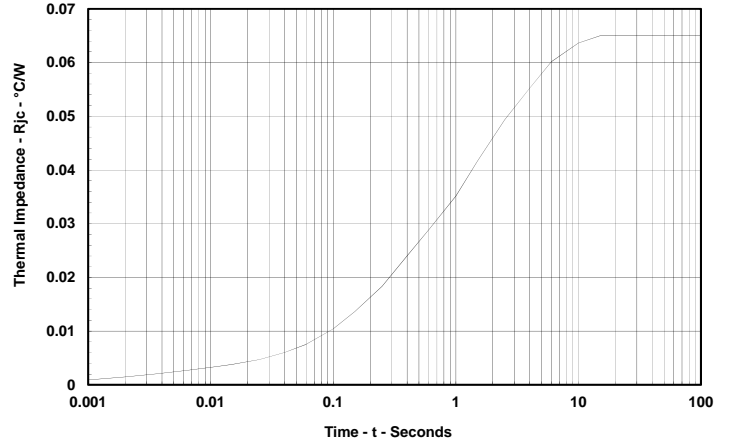
Thermal Characteristics

Characteristics	Symbol		Max.	Units
Thermal Resistance, Junction to Case	R _{θJ-C}	Per Module, both conducting	0.0325	°C/W
		Per Junction, both conducting	0.0650	°C/W
Thermal Impedance Coefficients	Z _{θJ-C}	Z _{θJ-C} = K ₁ (1-exp(-t/τ ₁))	K ₁ = 7.42E-04	τ ₁ = 3.33E-04
		+ K ₂ (1-exp(-t/τ ₂))	K ₂ = 9.52E-04	τ ₂ = 4.74E-03
		+ K ₃ (1-exp(-t/τ ₃))	K ₃ = 1.02E-02	τ ₃ = 9.60E-02
		+ K ₄ (1-exp(-t/τ ₄))	K ₄ = 5.23E-02	τ ₄ = 1.719
Thermal Resistance, Case to Sink Lubricated	R _{θC-S}	Per Module	0.01	°C/W

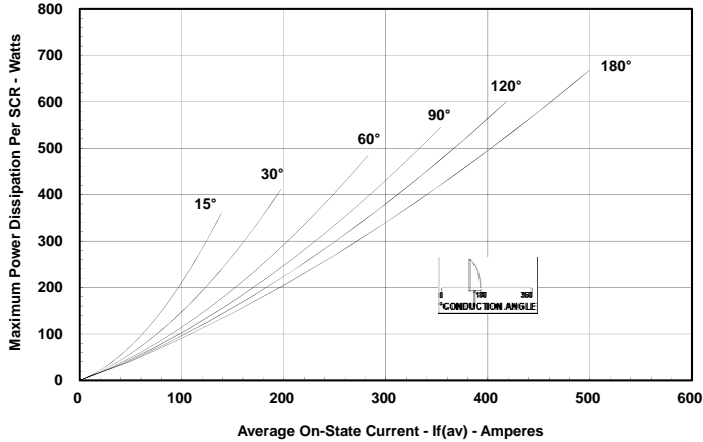
Maximum On-State Forward Voltage Drop
($T_j = 130^\circ\text{C}$)



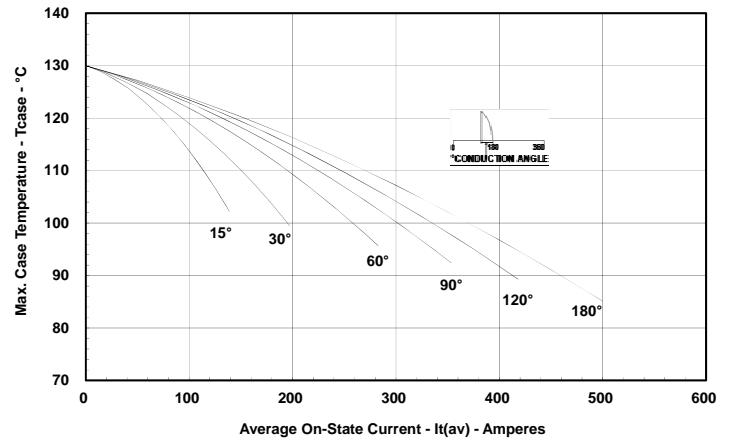
Maximum Transient Thermal Impedance
(Junction to Case)



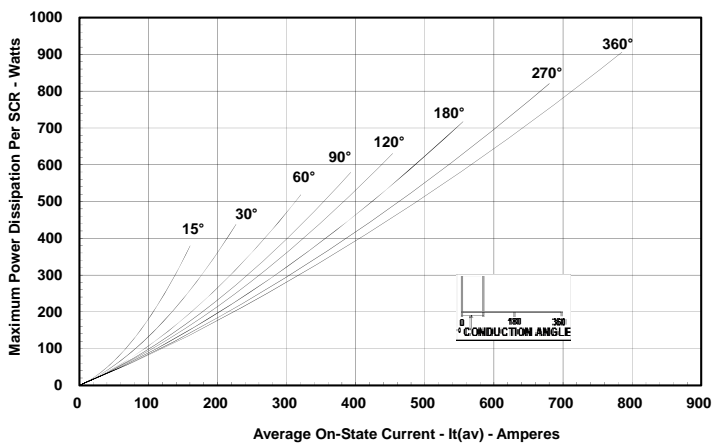
Maximum On-State Power Dissipation
(Sinusoidal Waveform)



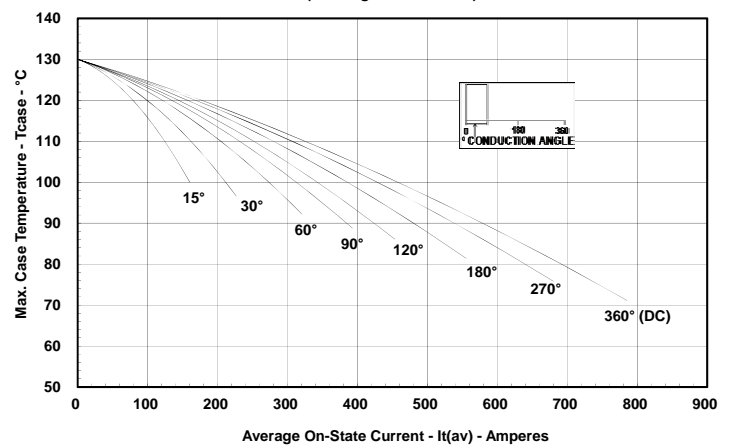
Maximum Allowable Case Temperature
(Sinusoidal Waveform)



Maximum On-State Power Dissipation
(Rectangular Waveform)



Maximum Allowable Case Temperature
(Rectangular Waveform)



Lead Kits

The LDR3 modules are supplied with a standard gate lead kit.

1. **Wire Composition**

FEP insulation rated to 200°C.

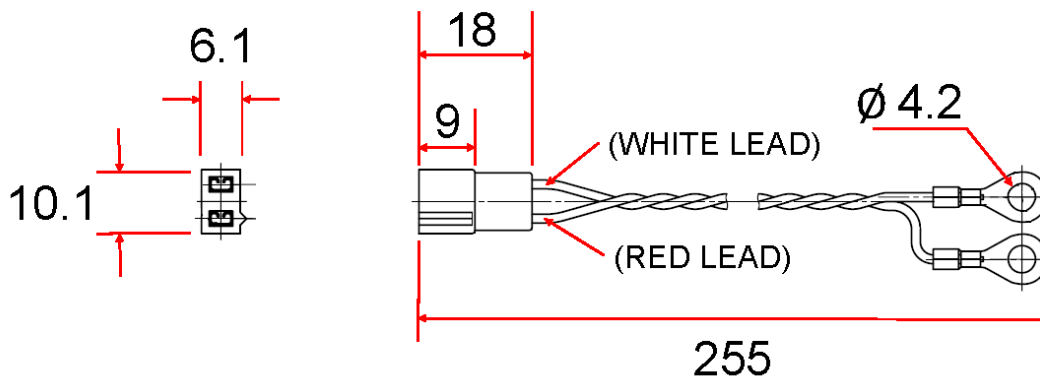
2. **Lead Colors**

Red (cathode) and White (gate). Red lead is positioned next to the key on black polarized housing.

3. **Receptacles**

Female terminal fits 2.8 x 0.8 blades.

Control Lead Set #1 (Terminals 4 & 5)



Control Lead Set #2 (Terminals 6 & 7)

